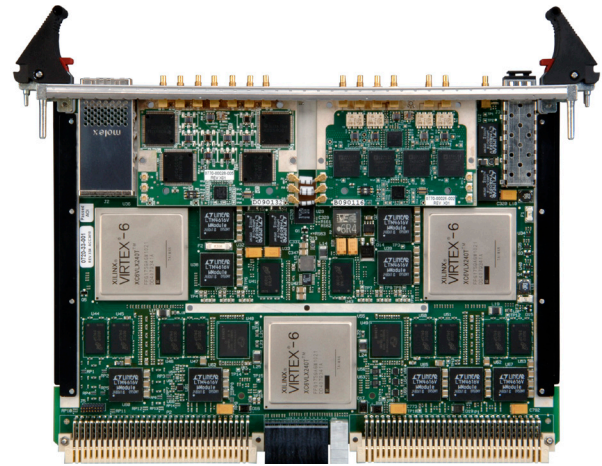


Titan-V6 VXS

Maximum FPGA Density
 Combined with High Performance
 Mixed Signal Technology.
 Without Compromise.



Features

Benefits

Eight Channels: Four 12-bit ADC Inputs at 1 GSPS each, Four 14-bit DAC Output at 1.2 GSPS Each	Achieves Ultra Low Latency From Acquisition to Response Critical to Jamming and Radar Decoy Applications
Sample Accurate Synchronization Across Multiple Boards	Enables Solutions for New Multi-channel Applications
ADC and DAC Can Use Common Clock	Synchronization Across Multiple Boards or Independent Clocks
Twelve Digital I/O Channels Running at Up to 6.4 Gb/s Using CXP Front Panel Connection	Flexible Data Movement Across the Front Panel For Use in Standard VME Environments
Dual 4x Full Duplex VXS Links and Two Full Duplex VITA 41.6 Ethernet Links	Enhanced VXS Capability
Three Xilinx Virtex®-6 devices (LX240, LX365, LX550, SX315, or SX475)	Matched FPGA Processing and Analog Data Bandwidth for Dense Channel-count Systems
Five GB DDR3 SDRAM Memory	Large Memory Resources for Application Flexibility
Advanced Temperature & Current Monitoring	Protection From Damage and Usable in Customer Applications
Comprehensive Developer's Kit Provided Including FPGA Interface Cores, QuiXstart FPGA Utilities, Software and Reference Design	Faster Application Development
Convection or Conduction Cooled Options	Ruggedization Designed in For Demanding Deployed Applications

Overview

The QuiXilica Titan-V6 VME / VXS is a 6U ANSI/VITA 41 (VXS) compliant high-speed digitizer board combining high density FPGA processing with four 12-bit A/D input channels at 1 GSPS (Gigasamples per second) and four 14-bit D/A output channels at 1.2 GSPS. By employing three Xilinx Virtex-6 FPGAs, Tekmicro's Titan-V6 offers unmatched FPGA processing density per channel making it ideal for high channel count signal processing in applications.

Titan-V6 Reduces System Size by 50%

The Titan-V6 includes four 1.0 GSPS analog input channels, four 1.2 GSPS analog output channels, and three Xilinx Virtex-6 FPGAs, providing up to 6,048 DSP slices and 3.6 TeraMAC/s of signal processing. Having ADC and DAC channels on a single board with high density FPGA processing, Titan-V6 can reduce the number of boards in a system by up to 50%. Titan-V6 transfers full sensor-rate data from the ADC processing (signal capture) to the DAC processing (waveform generation). This is an ideal solution for EW applications such as jammers and Radar decoys. The Titan-V6 features high bandwidth, low latency interconnect paths between its FPGAs. These have been carefully specified to ensure that data from the ADC input can be routed to the DAC output in support of low latency applications. Synchronization of ADC and DAC sampling on a

single board, and on multiple boards, is done using an external trigger signal. This offers significant throughput advantages for a range of advanced processing algorithms including multi-channel algorithms found in applications such as direction finding, STAP (Space Time Adaptive Processing) Radar, EW (jamming) and Synthetic Aperture Radar (SAR) Image Formation.

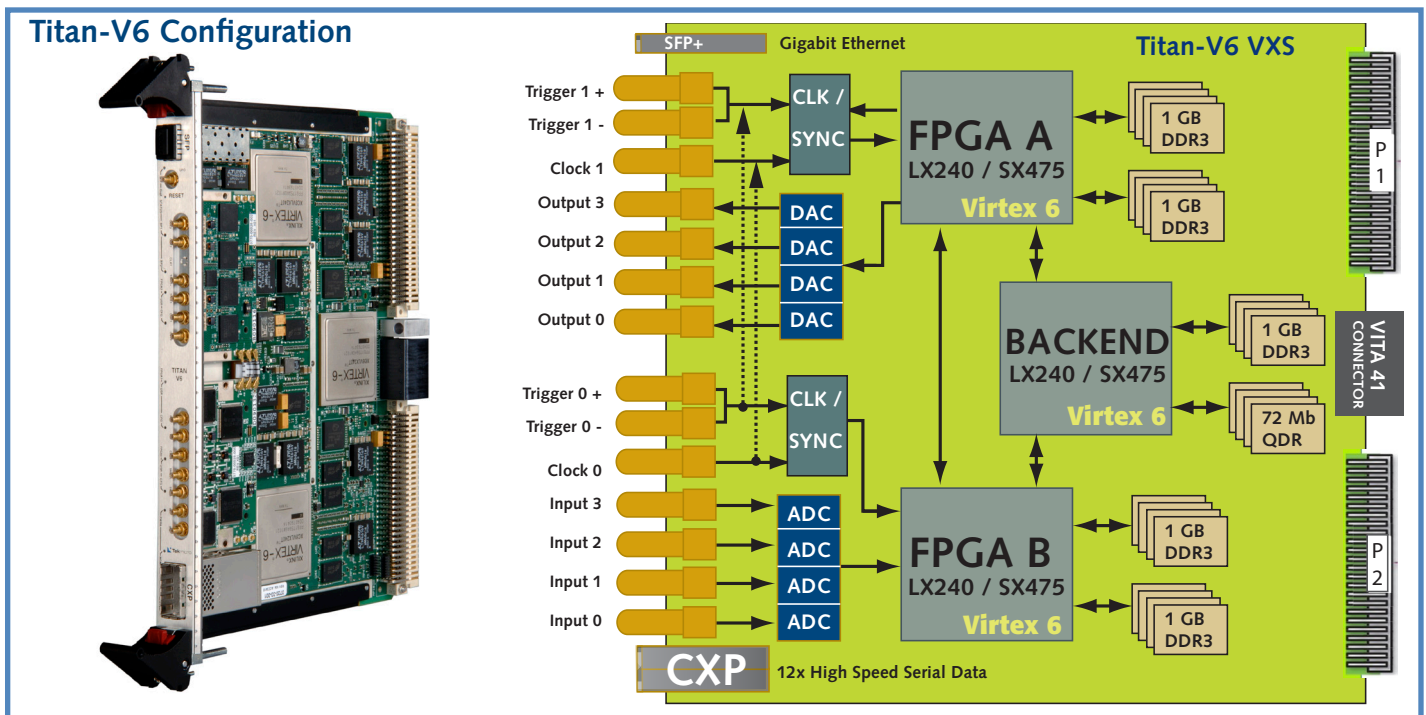
The Titan-V6 is available for a wide range of operating environments including commercial grade, rugged air, and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details see Tekmicro's Rugged Data Sheet.

In addition to Titan-V6, Tekmicro offers a broad range of Xilinx Virtex-6 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

Titan-V6 VXS Details

ADC

Four channels of 1.0 GSPS, 12-bit resolution analog to digital conversion is provided using the Texas Instruments ADS5400. The input is single-ended, AC coupled with a full scale input level of 10 dBm (2.0 V p-p) into 50 ohms.



DAC

Four channels of up to 1.2 GSPS, 14-bit resolution digital to analog conversion is provided using the Analog Devices' AD9736. The output is single-ended, AC coupled. Maximum full scale output is 4.5 dBm (1.1 V p-p) into 50 ohms.

Virtex-6 FPGAs

Xilinx Virtex-6 FPGAs are the heart of the Titan-V6. The FPGAs interface between the ADC's, memory and I/O resources to provide a platform for implementing high performance real time processing. The Titan-V6 is configured with three Xilinx Virtex-6 devices (LX240, LX365, LX550, SX315, or SX475). All FPGAs are interconnected by wide parallel LVDS busses and via high speed serial links using the Xilinx GTX transceivers.

Front Panel High Speed Serial I/O

One 12-fiber CXP site is provided on the front panel for standard protocols such as Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 & 17.2), and Fibre Channel.

VXS Backplane High Speed Serial I/O

The Titan-V6 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGA on the Titan-V6. A JTAG connection is available to allow users to configure the FPGA via standard Xilinx development tools. On board flash is available and can configure the FPGA on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGA through a Gigabit Ethernet link from a remote server after a power up or reset event.

Trigger

Trigger input connections are provided on the front panel to allow the hardware to be employed in a variety of Radar and EW scenarios. The trigger inputs are LVDS (LVPECL is a factory build option). One trigger input serves the DAC channels, and a second

serves the ADC channels, or a single trigger input can used for all eight analog IO channels. The trigger inputs may be used to synchronize multiple Titan-V6 boards to within a single sample period.

Clock

One clock input serves the four ADC channels, and a second clock input serves the four DAC channels, or all eight analog I/O channels may be clocked from a single clock input (factory build option). The minimum input clock level is -6 dBm into 50 ohms.

Memory

The Titan-V6 has two independent banks of on board double data rate (DDR3) SDRAM for each FPGA. The front end FPGAs have two 1 GB banks, each with throughput of 6.4 GB/s, while the back end FPGA has two 512 MB banks, each with throughput of 3.2 GB/s. The total memory capacity is 5 GB with aggregate throughput of 32 GB/s across six banks. All DDR3 memory banks are clocked at 400 MHz for an 800 MT/s transfer rate.

System Monitoring

The Titan-V6 includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection when the Titan-V6 is operating in different environmental scenarios. The output from the sensors is available to users' FPGA firmware applications, to allow the user application to adapt to changes in environmental conditions. The Titan-V6 also uses the system monitoring sensors to implement a system protection mechanism which will, independently of the users' application, prevent excessive current or temperature from damaging the board.

PERFORMANCE SPECIFICATIONS

A/D Converter

Quantity: 4

Sampling Rate: 1.0 GSPS

Resolution: 12-bits

Type: Texas Instruments ADS5400

Bandwidth: Up to 3rd Nyquist (1.5 GHz)

D/A Converter

Quantity: 4

Sampling Rate: 1.2 GSPS

Resolution: 14-bits

Type: Analog Devices AD9736

Bandwidth: 1st Nyquist

Front Panel Trigger Inputs

Quantity: 1 or 2 via (2 or 4) SSMC Connectors

Type: LVDS Termination: LVDS 100 Ω differential terminated. (LVPECL as factory build option).

Mode: Optional Independent trigger inputs for ADCs and DACs

Master/Slave: Single common trigger for both ADC and DAC

External Clock

Quantity: 1 or 2 each via SSMC Connector

Type: Single ended 50 Ω terminated

Input Power Range: 6 dBm (min) to 8 dBm (max)

Operating Modes: Clock Standalone / Master/Slave.

Memory

DDR3 SDRAM (2 fully independent banks per FPGA)

Size: 1 GB per front end bank, 512 GB total per back end bank

Bus Width: 64 bits per front end bank, 32 bits per back end bank

Speed: 400 MHz clock rate, 800 MT/s

Front Panel High Speed Serial Interface

12x Fiber Optic Transceivers on CXP module

Up to 6.4 Gb/s, 8B/10B or 64/66 encoding

Range of standard protocols, including Gigabit Ethernet and Serial FPDP.

Network Interface

Front panel SFP for fiber or copper Gigabit Ethernet

VITA 41.6 P0 interface for 1000BASE-KX Gigabit Ethernet

Onboard Gigabit Ethernet switch

JTAG Port

Access to Virtex-6 FPGAs is available via custom JTAG cable assembly that interfaces with the standard Xilinx JTAG programming cable.

Size: Standard 6U VMEbus board, single slot

Optional VXS P0 connector for backplane I/O

Power: +5V, +3.3V, \pm 12V from backplane. Power consumption is dependent on customer application. Power estimation model is provided as part of the Developers Kit.

Contact factory for additional performance details.

UNITRONIX Pty Ltd

PO Box 486, Morisset NSW 2264

NSW: Tel: 61 2 4977 3511 Fax: 61 2 4977 3522

WA: Tel: 61 8 9455 2424 Fax: 61 8 9455 2458

unitsyd@unitronix.com.au www.unitronix.com.au



TEK Microsystems Inc.

300 Apollo Drive

Chelmsford, MA 01824

voice +1.978.244.9200

fax: +1.978.328.5951

email: sales@tekmicro.com

www.tekmicro.com